

CS2082

Dual Airbag Deployment ASIC

The CS2082 controls and monitors two airbag firing loops. The independent firing loops are low- and high-side controlled. Device communication is through a Serial Peripheral Interface (SPI) port, and includes frame error detection circuitry for data reliability.

Diagnostics include squib resistance measurement and continuous monitoring for shorts to ground, shorts to battery, and for open loops. The high- and low-side drivers can be individually activated to guarantee function and to identify shorts between firing loops. Additional features include power on reset, overtemperature protection, a charge pump, high-side safing sensor closure detection, an analog multiplexer, a monitor to ensure battery potential, and a programmable monitor to ensure firing potential.

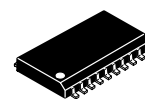
Features

- Serial Input Bus
- Two Squib Outputs
- Low- and High-Side Control
- Monitors
 - Squib Resistance
 - Short to Ground or Battery
 - Battery Potential
 - Firing Potential
- Safing Sensor Detection
- 60 V Peak Transient Voltage



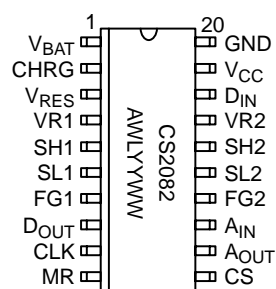
ON Semiconductor™

<http://onsemi.com>



SO-20L
DW SUFFIX
CASE 751D

PIN CONNECTIONS AND MARKING DIAGRAM



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
|--------------|---------|------------------|
| CS2082EDW20 | SO-20L | 37 Units/Rail |
| CS2082EDWR20 | SO-20L | 1000 Tape & Reel |

CS2082

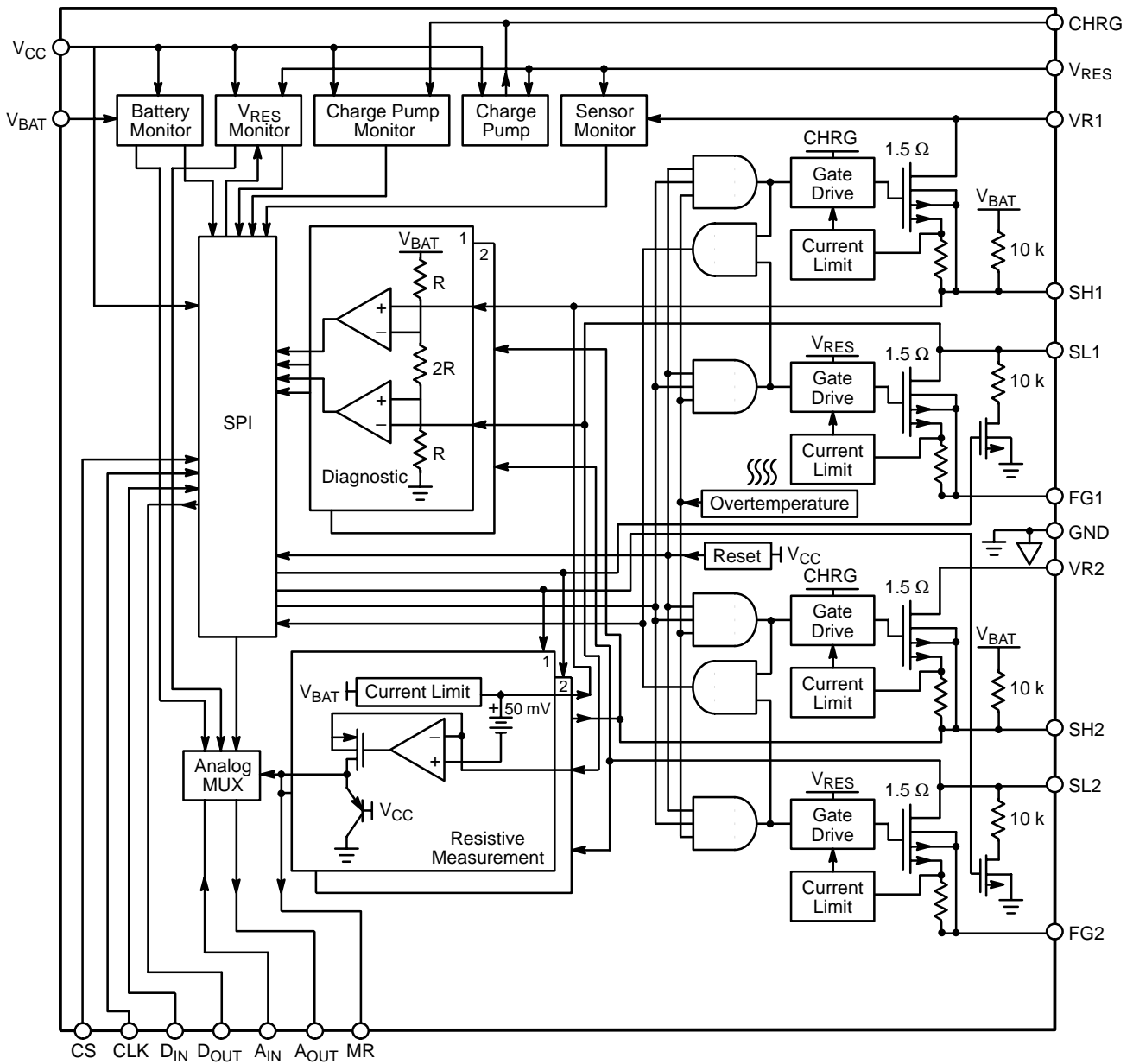


Figure 1. Block Diagram

MAXIMUM RATINGS*

| Rating | Value | Unit |
|--|------------------------------------|----------|
| Storage Temperature | -40 to 150 | °C |
| V _{BAT} | -0.3 to 24 | V |
| V _{RES} | -0.3 to 30 | V |
| V _{CC} | -0.3 to 6.0 | V |
| ESD Susceptibility (Human Body Model) | 500 | V |
| Power Dissipation (Non-Firing) | 0.15 | W |
| Power Dissipation (Both Firing Loops With Squibs Shorted) | 140 | W |
| Power Dissipation (Squib Resistance Measurement) | 1.6 | W |
| Peak Transient Voltage (46 V Load Dump @ 14 V V _{BAT}) | 60 | V |
| Lead Temperature Soldering: | Reflow: (SMD styles only) (Note 1) | 230 peak |

1. 60 second maximum above 183°C.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (4.75 V < V_{CC} < 5.25 V, 8.0 V < V_{RES} < 30 V, 9.0 V < V_{BAT} < 18 V, -40°C < T_A < +85°C; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|-----------|-----------------|-----|-----|-----|------|
|-----------|-----------------|-----|-----|-----|------|

Supply Requirements

| | | | | | |
|--------------------------------------|---|---|-----|-----|----|
| V _{CC} Quiescent Current | V _{CC} = 5.25 V | - | 2.0 | 4.0 | mA |
| V _{BAT} Quiescent Current | V _{BAT} = 18 V | - | 2.5 | 5.0 | mA |
| V _{BAT} Measurement Current | V _{BAT} = 18 V, R _{SQUIB} = 1.0 Ω | - | - | 80 | mA |
| V _{RES} Quiescent Current | V _{RES} = 30 V | - | - | 1.0 | mA |
| V _{RES} Firing Current | V _{RES} = 30 V | - | - | 3.0 | mA |

Power on Reset

V_{BAT} = 9.0 V, V_{RES} = 10 V

| | | | | | |
|----------------------------|-------------------------|------|------|------|----|
| Power Reset Active Voltage | V _{CC} Falling | 3.50 | 4.00 | 4.25 | V |
| Power Reset Off Voltage | V _{CC} Rising | 3.65 | 4.20 | 4.50 | V |
| Hysteresis | - | 50 | - | - | mV |

Low Side Driver

V_{RES} = 8.0 V = V_{RX}, V_{CC} = 5.0 V, V_{BAT} = 8.0 V

| | | | | | |
|-------------------------------------|--|-----|-----|-----|----|
| Saturation Voltage | I = 1.2 A | - | - | 1.8 | V |
| Current Limit (I _{LIMIT}) | V _{SLX} - V _{FGX} = 5.0 V | 1.2 | 1.6 | 2.0 | A |
| Turn-on Delay Time | From CS falling Edge, I _D = 0.9 × I _{LIMIT(MIN)} | - | - | 75 | μs |
| Turn-off Delay Time | From CS falling Edge, I _D = 0.1 × I _{LIMIT(MIN)} | - | - | 25 | μs |

High Side Driver

V_{RES} = 8.0 V = V_{RX}, V_{CC} = 5.0 V, V_{BAT} = 8.0 V

| | | | | | |
|---|--|-----|-----|-----|----|
| Saturation Voltage | I = 1.2 A | - | - | 1.8 | V |
| Current Limit (I _{LIMIT}) | V _{RX} - V _{SHX} = 5.0 V | 1.2 | 2.0 | 2.5 | A |
| V _{R1} Quiescent Current Drivers off | V _{RX} = V _{RES} = 30 V | - | - | 1.0 | mA |
| V _{R2} Quiescent Current Drivers off | V _{RX} = V _{RES} = 30 V | - | - | 100 | μA |
| Turn-on Delay Time | From CS falling Edge, I _D = 0.9 × I _{LIMIT(MIN)} | - | - | 100 | μs |
| Turn-off Delay Time | From CS falling Edge, I _D = 0.1 × I _{LIMIT(MIN)} | - | - | 25 | μs |

Thermal Shut Down

| | | | | | |
|-----------------------|----------------------|-----|-----|-----|----|
| Thermal Shutdown Temp | Guaranteed by Design | 150 | 180 | 210 | °C |
| Thermal Hysteresis | Guaranteed by Design | 30 | 40 | 60 | °C |

CS2082

ELECTRICAL CHARACTERISTICS (continued) (4.75 V < V_{CC} < 5.25 V, 8.0 V < V_{RES} < 30 V, 9.0 V < V_{BAT} < 18 V, -40°C < T_A < +85°C; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|--|-------------------------|-------------------------|-------------------------|----------|
| Thermal Shut Down | | | | | |
| Time to Thermal Shutdown | R _{SQUIB} = 0, V _{RX} = 30 V, T = 85°C, Guaranteed by Design | 7.0 | – | – | ms |
| Squib Resistive Measurements V _{CC} = 5.0 V, R _{MR} = 49.9 Ω, V _{RES} = 30 V | | | | | |
| Squib Differential Voltage | V _{DIFF} = SHx – SLx, R _{SQUIB} = 1.0 Ω to 10 Ω | 46 | 53 | 60 | mV |
| Difference Between SHx & MR current – SHx reference | I _{SQUIB} = 50 mA | –1.0 | – | 1.0 | % |
| SHx Current Limit | R _{SQUIB} = 0 | 67 | 100 | 133 | mA |
| SLx Current Limit | R _{MR} = 0 | 77 | 115 | 153 | mA |
| MR Voltage Clamp | – | V _{CC} – 0.3 | – | V _{CC} + 0.3 | V |
| Turn On Delay Time excluding external Capacitors | – | – | – | 100 | μs |
| Turn off Delay Time | – | – | – | 50 | μs |
| Short Measurements V _{CC} = 5.0 V, V _{RES} ≥ V _{BAT} , V _{RX} ≥ V _{BAT} | | | | | |
| SHx pull-up resistance to V _{BAT} SLx pull-down resistance | V _{BAT} = 18 V | 4.0 4.0 | 10 10 | 17 17 | kΩ kΩ |
| Pull-up resistor matching | – | –5.0 | – | 5.0 | % |
| Pull-down resistor matching | – | –5.0 | – | 5.0 | % |
| Short to V _{BAT} Trip | SHx short to Battery SLx bit set to 1 | 0.73 × V _{BAT} | 0.75 × V _{BAT} | 0.77 × V _{BAT} | V |
| Short to GND Trip | SHx short to GND SGx bit set to 1 | 0.23 × V _{BAT} | 0.25 × V _{BAT} | 0.27 × V _{BAT} | V |
| V_{BAT} Monitoring V _{CC} = 5.0 V, External V _{BAT} Diode not included, V _{RES} = 30 V | | | | | |
| V _{BAT} Low Trip | BL bit set to 1 when below trip | 7.5 | 8.5 | 9.5 | V |
| V _{BAT} High Trip | BL bit set to 0 when above trip | 8.0 | 9.0 | 10 | V |
| V_{RES} Monitoring V _{CC} = 5.0 V, V _{BAT} = 18 V | | | | | |
| V _{RES} Low Trip | \$6d AUX register b0 = 0 | 15.7 | 17.5 | 19.3 | V |
| V _{RES} High Trip | \$6d AUX register b0 = 0 | 16.5 | 18.5 | 20.5 | V |
| V _{RES} Low Trip | \$6d AUX register b0 = 1 | 21.5 | 24.0 | 26.5 | V |
| V _{RES} High Trip | \$6d AUX register b0 = 1 | 22.5 | 25 | 27.5 | V |
| Safing Sensor Monitor | | | | | |
| External Resistance Trip Range | SSC bit set when resistance is less | 30 | 400 | 600 | Ω |
| Charge Pump and Monitor V _{CC} = 5.0 V, V _{BAT} = 10 V | | | | | |
| Oscillator Frequency | V _{RES} = 10 V | 200 | – | 800 | kHz |
| Charge Pump charge time | C _{CHG} = 0.1 μF, V _{RES} = 8.0 V, Chrg from 8.0 V to 14 V | – | – | 20 | ms |
| Charge Pump Low Voltage | CL bit set to 1 when below trip | 14.5 | 16.0 | 17.5 | V |
| Charge Pump High Voltage | CL bit set to 0 when above trip | 15.0 | 17.5 | 18.0 | V |
| Analog MUX V _{CC} = 5.0 V | | | | | |
| A _{OUT} Output Range | – | 0.1 | – | V _{CC} – 0.1 | V |
| A _{IN} Input Range | – | 0 | – | V _{CC} | V |

CS2082

ELECTRICAL CHARACTERISTICS (continued) (4.75 V < V_{CC} < 5.25 V, 8.0 V < V_{RES} < 30 V, 9.0 V < V_{BAT} < 18 V, -40°C < T_A < +85°C; unless otherwise stated.)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---------------------------|-----|------|------|------|
| Analog MUX V _{CC} = 5.0 V | | | | | |
| MUX internal voltage drop | I _{OUT} = 100 μA | – | – | 100 | mV |
| Proportion of V _{BAT} on A _{OUT} with V _{BAT} selected | – | 23 | 25 | 27 | % |
| A _{OUT} Impedance with V _{BAT} selected | – | 6.0 | 15.0 | 35 | kΩ |
| Proportion of V _{RES} on A _{OUT} with V _{RES} selected | – | 15 | 17 | 19 | % |
| A _{OUT} Impedance with V _{RES} selected | – | 6.0 | 12.5 | 25.5 | kΩ |

| | | | | | |
|--|---|-----------------------|-----|-----------------------|----|
| Digital Inputs – D_{IN}, CLK, CS V _{CC} = 5.25 V, V _{BAT} = 18 V, V _{RES} = 30 V | | | | | |
| Input Low Voltage (V _{IL}) | – | 0 | – | 0.3 × V _{CC} | V |
| Input High Voltage (V _{IH}) | – | 0.7 × V _{CC} | – | V _{CC} | V |
| Input Voltage Hysteresis | – | 100 | – | – | mV |
| Input Pull Down Current (I _{IH}) | – | 50 | 100 | 200 | μA |

| | | | | | |
|---|------------------------------|------------------------|-----|-----|----|
| Digital Outputs – D_{OUT} V _{CC} = 4.75 V, V _{BAT} = 18 V, V _{RES} = 30 V | | | | | |
| Output Low Voltage (V _{OL}) | I _{SINK} = 1.0 mA | – | – | 0.4 | V |
| Output High Voltage (V _{OH}) | I _{SOURCE} = 1.0 mA | V _{CC} – 0.75 | – | – | V |
| Tri-State Pull-up Current | CS = 0, D _{OUT} = 0 | 50 | 100 | 200 | μA |
| Rise Fall Time | C _{LOAD} = 200 pF | – | – | 50 | ns |

PACKAGE PIN DESCRIPTION

| Package Lead Number | Pin Symbol | Function |
|---------------------|------------------|----------------------------------|
| SO-20L | | |
| 1 | V _{BAT} | Battery Supply Voltage. |
| 2 | CHRG | Charge pump Storage. |
| 3 | V _{RES} | Reserve Supply Voltage. |
| 4 | VR1 | Loop 1 Supply. |
| 5 | SH1 | Squib 1 High Side. |
| 6 | SL1 | Squib 1 Low Side. |
| 7 | FG1 | Loop 1 Return. |
| 8 | D _{OUT} | Serial Port output. |
| 9 | CLK | Serial Port Clock. |
| 10 | MR | Squib Resistance Output Current. |
| 11 | CS | Serial Port Chip Select. |
| 12 | A _{OUT} | Analog MUX Output. |
| 13 | A _{IN} | Analog MUX Input. |
| 14 | FG2 | Loop 2 Return. |
| 15 | SL2 | Squib 2 Low Side. |
| 16 | SH2 | Squib 2 High Side. |
| 17 | VR2 | Loop 2 Supply. |

PACKAGE PIN DESCRIPTION (continued)

| Package Lead Number | Pin Symbol | Function |
|---------------------|-----------------|-------------------------|
| SO-20L | | |
| 18 | D _{IN} | Serial Port Input. |
| 19 | V _{CC} | 5.0 V Regulated Supply. |
| 20 | GND | Signal Ground. |

FUNCTIONAL DESCRIPTION

The CS2082 is an automotive air bag deployment and diagnostic system for up to two independent firing loops. Communication with the ASIC is through a synchronous serial port using Serial Peripheral Interface (SPI) protocol, at CLK rates up to 2.0 MHz.

Data is simultaneously sent from the D_{OUT} pin and received at the D_{IN} pin under the control of the CS and CLK pins. Error detection logic is included in the SPI to guard against glitches on either the CS or CLK logic signal inputs. A valid CS frame must contain exactly 8 CLK cycles for each CS low-high-low transition. Detection of a frame error will cause input data for that frame to be ignored and an error code (\$FE) to be sent during the next valid CS frame.

The data at D_{OUT} is sent MSB first and is guaranteed valid before the rising edge of CLK. The 8 bits sent from D_{OUT} after CS goes high will be the previous data received, data from either the status register or the fault register, or the CS frame error code (\$FE).

The data at D_{IN} is received MSB first and must be valid before the rising edge of CLK. The 8 bits received at D_{IN} before CS goes low will be the current command. Table 1 defines the legal 8-bit SPI commands, where d = four data bits and x = don't care. All other inputs will be ignored.

Table 1. Valid CS2082 SPI Commands

| COMMAND | FUNCTION |
|---------|-------------------------------|
| \$1x | Read Status Register |
| \$2x | Read Fault Register |
| \$3d | Squib Resistance Measurements |
| \$4d | Analog MUX Select |
| \$5d | Low Side Switch Control |
| \$6d | Auxiliary Control Register |
| \$Ad | High Side Switch Control |

Read Status Register – \$1x

The \$1x command causes the data contained in the status register to be sent from D_{OUT} during the next valid CS frame. The status register reports the condition of the firing paths, closure detection of an external safing switch between

the V_{RES} and VR1 pins, the state of the internal charge pump, and the state of external V_{BAT} and V_{RES} power supplies. The status register is an 8-bit active-high register with bit definition as shown in Table 2.

Table 2. Status Register Bit Definition

| BIT | VALUE | DESCRIPTION |
|-----|-------|--|
| D7 | 0 | Always Logic zero |
| D6 | 0 | Always Logic zero |
| D5 | F1 | SH1 and SL1 switches active |
| D4 | F2 | SH2 and SL2 switches active |
| D3 | SSC | Safing Sensor is closed |
| D2 | RL | V _{RES} voltage is below trip |
| D1 | BL | V _{BAT} voltage is below trip |
| D0 | CL | CHRG voltage is below trip |

Read Fault Register – \$2x

The \$2x command causes the data contained in the fault register to be sent from D_{OUT} during the next valid CS frame. The register reports fire path faults by continuously comparing each path to a portion of the voltage at the V_{BAT} pin. The fault register is an 8-bit active-high register with bit definition as shown in Table 3.

Table 3. Fault Register Bit Definition

| BIT | VALUE | DESCRIPTION |
|-----|-------|---|
| D7 | 0 | Always Logic zero |
| D6 | 0 | Always Logic zero |
| D5 | 0 | Always Logic zero |
| D4 | 0 | Always Logic zero |
| D3 | SB2 | High Side of Sqib 2 above 75% V _{BAT} trip threshold |
| D2 | SB1 | High Side of Sqib 1 above 75% V _{BAT} trip threshold |
| D1 | SG2 | Low Side of Sqib 2 below 25% V _{BAT} trip threshold |
| D0 | SG1 | Low Side of Sqib 1 below 25% V _{BAT} trip threshold |

Each SHx pin is pulled up to V_{BAT} while each SLx pin is pulled down to GND through separate nominal 10 kΩ resistors, thus biasing each normal fire path to about 1/2 V_{BAT}. An open fire path has been detected if both the SBx and SGx bits are set for that path. To detect faults between fire paths and to test driver function, each driver should be activated individually. The activated driver should cause its respective fault bit to be set. If an activated driver does not set its respective fault bit, a driver fault has been detected. If an activated driver causes the fault bit of an inactivated driver to be set, a fault *between* fire paths has been detected. Table 4 defines the implied ranges over which the various types of faults can be detected.

Table 4. Implied Resistive Fault Detection Ranges

| Fault | Min | Nom | Max | Unit |
|------------------|-----|-----|-----|------|
| Short to Ground | 1 | 5 | 10 | kΩ |
| Short to Battery | 1 | 5 | 10 | kΩ |
| Open | 5 | 20 | 40 | kΩ |
| Driver Open | 1 | 5 | 10 | kΩ |
| Driver Shorted | 1 | 5 | 10 | kΩ |
| Squib to Squib | 1 | 5 | 10 | kΩ |

Squib Resistance Measurement – §3d

The §3d command activates squib resistance measurement for the selected firing path. The respective active-high bit definitions are shown in Table 5. At power-up, the default path is 'None.'

Table 5. Squib Resistance Path Select

| D3 | D2 | D1 | D0 | Path |
|----|----|----|----|---------|
| x | x | 0 | 0 | NONE |
| x | x | 0 | 1 | SQUIB 1 |
| x | x | 1 | 0 | SQUIB 2 |
| x | x | 1 | 1 | NONE |

Squib resistance is measured by forcing 50 mV nominal (proportional to V_{CC}) across the squib. The resulting squib current is passed to an external load resistor at the MR pin, converting the current back into a voltage. This voltage may be read directly at the MR pin, or passed through the analog multiplexer to be read at the A_{OUT} pin. The known values of the squib differential voltage (V_{DIFF}) and the MR resistance (R_{MR}), and the measured MR voltage (V_{MR}) indicate squib resistance such that:

$$RSQUIB = \frac{RMR \times V_{DIFF}}{V_{MR}}$$

Typical MR voltage response for R_{MR} = 50 Ω over a squib resistance range of 0.6 Ω to 6.0 Ω is illustrated in Figure 2.

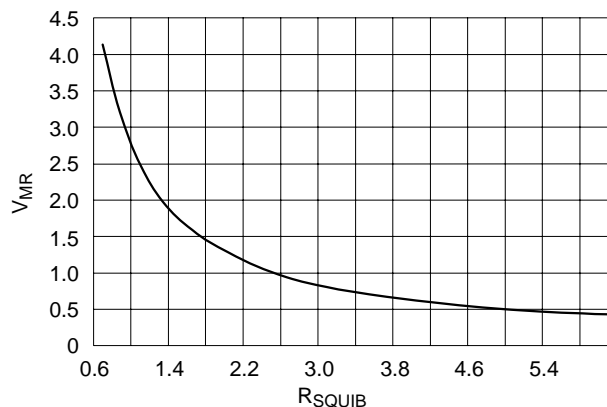


Figure 2. Typical MR Voltage Response

Measurement accuracy of the CS2082 with combined tolerances and with an external 1% load resistor at the MR pin can be defined by the equation:

$$RSQ(E) = \frac{V_{DIFF(IDEAL)} \times R_{MR(IDEAL)}}{\left(\frac{V_{DIFF \pm 12\%}}{R_{SQ(A)}}\right) \pm 1\% \times R_{MR} \pm 1\%}$$

$$= RSQ(A) + 12.5\% / -15.94\%$$

where V_{DIFF(IDEAL)} and R_{MR(IDEAL)} are the assumed values for the squib resistance solution algorithm, R_{SQ(A)} is the actual squib resistance, and R_{SQ(E)} is the result of the solution algorithm. An additional error may be added if the MR voltage is measured through the analog multiplexer.

In operation, current is sourced from V_{BAT} to the SHx pin, through the squib to the SLx pin, and returned to ground through the MR load resistor. Current clamps are provided for both the SHx and SLx pins and a voltage clamp is provided for the MR pin. These clamps along with the resolution of the ADC are the constraining factors for the minimum and maximum measurable squib resistance values.

The minimum measurable squib resistance can be defined as:

$$\frac{V_{DIFF(MIN)}}{I_{LIM(MAX)}} \leq RSQUIB(MIN) \leq \frac{V_{DIFF(MIN)} \times R_{MR(MIN)}}{V_{CLAMP(MAX)}}$$

The maximum measurable squib resistance can be defined as:

$$RSQUIB(MAX) = \frac{V_{DIFF(MAX)} \times R_{MR(MAX)} \times (2^n - 1)}{V_{CC(MIN)}}$$

In the above equations, V_{DIFF} is the SHx–SLx forced differential voltage, I_{LIM} is the SHx resistive measure current limit, V_{CLAMP} is the MR clamp voltage, R_{MR} is the toleranced MR load resistor value and n is the number of bits of resolution of the ADC.

It should be noted that during resistive measurements, faults to GND or BAT (dependent on V_{BAT} voltage and

squib resistance) may be reported by the fault register and should be ignored.

Power Dissipation during resistive measurement can be calculated as:

$$P = I_{SQUIB}(V_{BAT} - V_{DIFF}) - (I_{SQUIB} \times R_{MR})$$

where V_{BAT} is the voltage at the CS2082 V_{BAT} pin and I_{SQUIB} is the measurement current through the squib. A typical value for P is 300 mW when $V_{BAT} = 13.5$, $V_{DIFF} = 50$ mV, $R_{SQUIB} = 2.0 \Omega$ and $R_{MR} = 49.9 \Omega$.

The resultant increase in power dissipation will cause a corresponding increase in die temperature which will cause a corresponding decrease in time to thermal shutdown of the CS2082. To minimize the impact of squib resistive measurements on time to thermal shutdown a 5% duty cycle is recommended.

Analog MUX – \$4d

The \$4d command selects one of five states at the A_{OUT} pin. The states are: High-Z; MR voltage; A_{IN} voltage; proportion of V_{BAT} ; proportion of V_{RES} . The active-high Analog Mux select register bit definitions are shown in Table 6. All other states will be interpreted as High-Z. At power-up, the default state is ‘High-Z.’

Table 6. Analog MUX Output Select

| D3 | D2 | D1 | D0 | State |
|----|----|----|----|----------|
| 0 | 0 | 0 | 0 | High-Z |
| 0 | 0 | 0 | 1 | MR |
| 0 | 0 | 1 | 0 | A_{IN} |
| 0 | 1 | 0 | 0 | BAT |
| 1 | 0 | 0 | 0 | RES |

Low Side Switch Control – \$5d

The \$5d command activates the low side switches. When a data bit is low that switch is turned on. More than one switch can be activated at a time. Bit assignment is shown in Table 7. At power-up, no switches are active.

Table 7. Low Side Switch Select

| D3 | D2 | D1 | D0 | Active |
|----|----|----|----|--------|
| x | x | 0 | 0 | BOTH |
| x | x | 0 | 1 | SL2 |
| x | x | 1 | 0 | SL1 |
| x | x | 1 | 1 | NONE |

Auxiliary Control Register – \$6d

The \$6d command selects the V_{RES} Monitoring trip threshold. The threshold determines when the \$1x Status Register reports $V_{RES} = 1$. Bit assignment is shown in Table 8. At power-up, default trip is 17 V.

Table 8. V_{RES} Monitor Trip Select

| D3 | D2 | D1 | D0 | Trip |
|----|----|----|----|------|
| x | x | x | 0 | 17 V |
| x | x | x | 1 | 23 V |

High Side Switch Control – \$Ad

The \$Ad command activates the high side switches. When a data bit is high, that switch is turned on. More than one switch can be activated at a time. Bit assignment is shown in Table 9. Note that the \$5d and \$Ad commands are binary complements, i.e., by sending 1010xx11, both high side switches are activated, and by sending the complement 0101xx00, both low side switches are activated. At power-up, no switches are active.

Table 9. High Side Switch Select

| D3 | D2 | D1 | D0 | Active |
|----|----|----|----|--------|
| x | x | 0 | 0 | NONE |
| x | x | 0 | 1 | SH1 |
| x | x | 1 | 0 | SH2 |
| x | x | 1 | 1 | BOTH |

CS2082

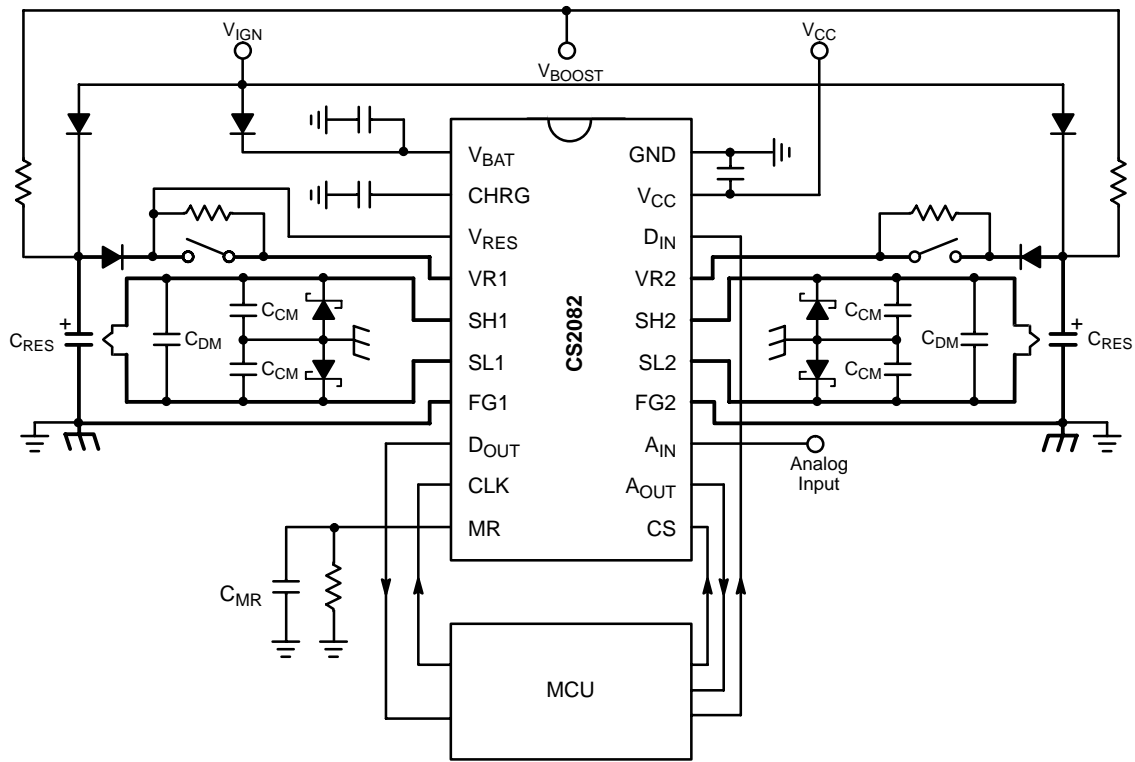
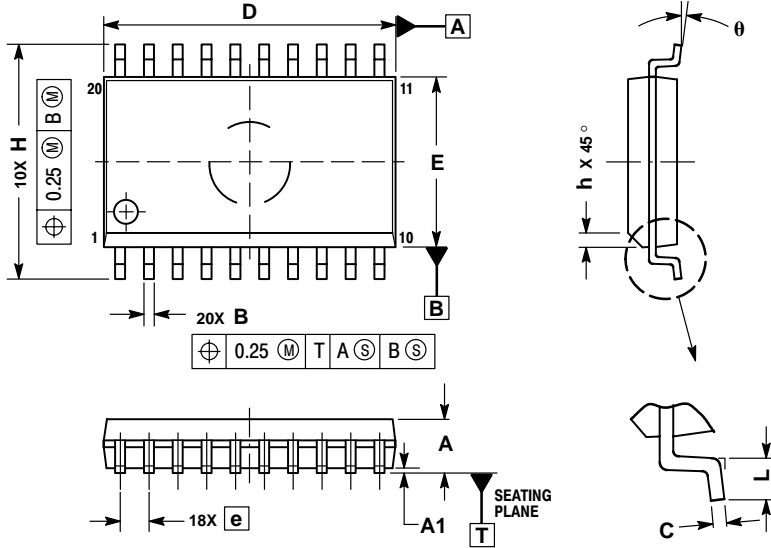


Figure 3. Application Diagram

CS2082

PACKAGE DIMENSIONS

SO-20L
DW SUFFIX
CASE 751D-05
ISSUE F



NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-----|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| θ | 0° | 7° |

PACKAGE THERMAL DATA

| Parameter | | SO-20L | Unit |
|------------------|---------|--------|------|
| R _{θJC} | Typical | 17 | °C/W |
| R _{θJA} | Typical | 90 | °C/W |

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031
Phone: 81-3-5740-2700
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.